IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Edward C. Douglas	Art Unit:	2827
Serial No.:	09/925,798	Examiner:	Alonzo Chambliss
Filed:	August 9, 2001		
Title:	INTEGRATED CIRCUIT PACKAGE		
Attorney Docket No.:	RTN2-019AUS		

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April 11 2002
Date of Signature and Mail Deposit

By: Anna Maria Keel
Anna Maria Keel

BOX NON-FEE AMENDMENT
Commissioner of Patents
Washington, D.C. 20231

Dear Sir:

RESPONSE

In response to the Office Action mailed January 31, 2002, please amend the application as follows:

In the Title:

Please change the Title to:

--METHOD FOR FABRICATING AN INTEGRATED CIRCUIT PACKAGE--

In the Specification:

Replace the paragraph on Page 7 beginning at line 26 with:

B2

Next, considering an exemplary one of the sites 40, and referring to FIGS. 2B and 2D′, each one of the plurality of the dielectric members 22_1 is disposed over, and affixed to, a corresponding one of the sites 40 using epoxy 24, as shown. More particularly, the dielectric members 22_1 are affixed to the platform 20 and portions of the electrical leads 16. It is noted that the dielectric members 22_1 includes a recess, or ridge 23, having side walls 25. Such configuration is provided to increase the surface tension between the applied B-stage epoxy 24 and the dielectric member 22_1 thereby to prevent the liquid-like epoxy from dripping off of the dielectric member 22_1.

In the Claims:

A clean copy of the claims is presented below a comparison between such claims and the previous claims is attached hereto in an appendix

Please cancel claim 11.

B3

12. (Amended) A method for packaging integrated circuit chips, comprising the steps of:

providing a lead frame having a plurality of sites therein, each site having electrical leads extending outwardly from an inner region of the site;

adhesively affixing each one of a plurality of plastic base sections over a corresponding one of the site;

connecting electrical wires between integrated circuit chips to be packaged at each one of the plurality of sites and the electrical leads at the corresponding one of the sites; and

adhesively affixing covers to encapsulate each one of the integrated circuit chips and the electrical wires connected thereto within cavities formed by the corresponding one of the plurality of the affixed covers and a corresponding one of the base sections.

B4

14. (Amended) The method recited in claim 12, comprising the steps of:

electrically connecting a conductive member of a base section to a bottom ground plane conductor of the integrated circuit chips with apertured dielectrics disposed between the sites of the lead frame and the conductive members and the with the apertures being in registration with the a corresponding one of the integrated circuit chips;

and wherein the affixing comprises affixing the plastic covers to provide packages

for the integrated circuit chips with such integrated circuit chips being disposed within cavities formed by the affixed cover and with a portion of the electrically conductive member being exposed exteriorly of the package.

Please cancel claim 15.

Please add the following new claims:

17. A method for package for an integrated circuit chip, comprising:

providing an electrically conductive lead frame having electrical leads extending outwardly from an inner region;

providing an adhesive material;

providing a base section having a top surface;

affixing a portion of the top surface to a bottom surface portion of the lead frame with the adhesive material, with portions of the electrical leads extending outwardly from the base section; and

providing a plastic cover over the base section, the plastic cover having a bottom surface, a portion of the bottom surface affixed to a top surface portion of the lead frame by the adhesive material, the base section and the cover being configured to provide a cavity when the cover and the base section are affixed with the integrated circuit chip being encapsulated within the provided cavity and

wherein during the affixing of the cover to the lead frame, the adhesive material extends into the cavity along a first direction and is confined within outer surface of

sidewalls of such cover along an opposite direction by inner surfaces of said sidewalls of such cover and,

wherein the cover is provided with a recess disposed within sidewalls and wherein during the affixing, ends of the sidewalls are affixed to the base section with the recess being in each one of the ends of the sidewalls, and with such recess having bottom surface and a rear surface to hold the adhesive material allowing a portion of the adhesive material to extend beyond the bottom surface into the cavity along a first direction while the rear surface of such recess retains such adhesive material within the sidewalls of the cover as such material is urged along an opposite direction.

18. The method recited in claim 17 including providing the cover with a ridge disposed along ends of sidewalls of the cover; and including disposing the adhesive material in the ridge between the cover and the lead frame to affix the cover to the lead frame.

In the Drawings:

Proposed changes top the drawings are attached hereto. The proposed changes are indicated in red. Approval is hereby requested.

REMARKS

The above-identified patent application has been amended and re-examination and reconsideration are hereby requested.

Proposed drawing changes are made in red. Approval is hereby requested.

Applicant has attempted to correct errors found by the Examiner and presented in paragraph 4 of the Office Action. HOWEVER, Applicant does not understand the objection raised in paragraph 5. In reviewing the specification, numeral 28 refers to the B-stage epoxy and numeral 32 refers to the sidewalls. Applicant's examination of the FIGS. finds this designation consistent with the FIGS. Applicant respectfully requested further explanation in order to comply with Examiner's request.

The rejection under 35 USC has been noted and the claims have been amended accordingly. It is respectfully submitted that the claims as now presented for examination are in accordance with 35 USC 112, second paragraph.

Claim 12 stands rejected under 35 USC 103 as being unpatentable over Brathwaite et al., in view of Rosenstock. Examiner takes the position that to form a plurality of sites is a duplication of parts and therefore has no patentable significance. Examiner cites In re Harza. In re Harza, however, deals with a block having a plurality of ribs and the prior art had one rib. The Court found no patentable significance to having additional ribs, over the prior art, absent an unexpected result. Applicant on the other hand is claiming in claim 12 a method for packaging integrated circuits by packing the chips while the chips are still on the lead frame; i.e., prior to them being separated. That is, the covers are placed over the chips, which themselves are still on the lead frame, prior to the chips being separated from the lead frame. Applicant forms a lead frame with a plurality of sites and then places the chips on sites of the lead frame and then merely places covers over the chips prior to their separation. Thus, Applicant has a way of

packaging a plurality of chips easier than by packaging each individual chip. Nothing in the applied references suggests or recognizes this easy way of packaging a plurality of chips. It is respectfully submitted therefore that the rejection of having duplication of parts is not applicable to the improved METHOD claimed by the Applicant.

New claims have been added to more fully distinguish Applicant's invention from the applied art.

Applicant submits that all of the claims are now in condition for allowance, which action is requested. Please apply any other charges or credits to Deposit Account No. 50-0845.

Respectfully submitted,

Date: 4/11/02

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Attachment: Sheets Showing Changes Made

rtn2-019aus- response to office action